PWB via) or a series connected inductance Ls (such as a series connected PWB via connector pin). The nominal impedance of the signal transmission line is Zo with a nominal delay of Do. The invention allows for a general mathematical solution to calculate the exact amount of transmission line propagation delay of a correcting transmission line to cancel out the impedance discontinuity caused by the reactive parasitic element.

For the correction of a parallel connected parasitic capacitive load the correcting transmission line impedance (Zc) will need to be higher than the normal impedance in the circuit (Zo) and of a delay Tc= (Zc·Cp) /((Zc/Zo)^2-1). For the correction of a parasitic series inductance the correcting impedance Zc will need to be lower than the normal impedance in the circuit and of a delay Tc= (Ls/Zc) /((Zo/Zc)^2-1). When applied properly, the impedance Zc is "loaded down" to Zo by a parasitic capacitance Cp or Zc is "raised up" to Zo by the parasitic inductance Ls. The control of the impedance mismatch comes at a price. There is a known time delay introduced by the correcting transmission line. This will be the value of Tc (the intrinsic unloaded delay of the Zc transmission media) times the ratio of Zc/Zo for capacitive parasitic cancellation or Tc times the ratio of Zo/Zc for inductive parasitic cancellation. This non-intrinsic delay penalty shall be called Tc'. For high frequency applications (fast edge rates) the value of Zc should not be close to Zo to minimize the value of Tc' which should not exceed one-half the edge rate of the signal involved if parasitic cancellation is to be effective.

The correcting transmission line of impedance Zc and delay Dc could be any conveniently allowed transmission line impedance, speed, and form factor (coaxial,

twisted, etc.). The general application can be created on a printed wiring board by etching the correcting transmission line at the same time that the normal signal impedance Zo is being etched. The will result in both transmission lines having the same propagation velocity (or unit delay Do) and there will be no additional time or cost involved. Higher impedances for Zc for capacitive parasitic cancellation can be traces etched narrower than the nominal impedance Zo and lower impedances for Zc can be etched wider than the nominal traces. The preferred implementation divides the calculated time of Tc, for the chosen impedance Zc, into two halves. Each half of Tc is placed on either side of the parallel capacitance of the series inductance.

With respect to Figure 1, it can be seen that the signal path is narrower before and after the parasitic capacitance Cp. The length of each narrow region is Tc/2. Each of the narrow regions has a chosen impedance Zc, while the thick regions of signal path have impedance Zo. Using the formulas as discussed above, the dimensions of the signal transmission path can therefore be customized to eliminate unwanted capacitance. Using conventional integrated circuit package signal transmission path designs, the present invention is able to compensate or eliminate up to 2.5 pF of capacitance for a signal with a rise time of 200 picoseconds.

Figure 2 shows a signal transmission path that has been designed to eliminate a series inductance Ls. In this example the necessary chosen impedance Zc is less than Zo so the signal path is made wider in the region adjacent both sides of the inductor Ls. Each side of the wide region of signal path is again Tc/2. For example

Figure 3 shows as a solution of the present invention, the custom routing provided in the ASIC package to provide impedance and cross-talk control. A further feature is to have the signals loop through the package so that it enters, brings the signal to the I/O structure of the die and continues on back out of the package toward the terminator mounted on the surface of the PWB. This allows for compensation on both sides of the load. Figure 3 shows the custom traces required to achieve the nominal Rambus impedance. The wide traces are the Rambus RSL lines and the narrow traces are the "regular" minimum width (35 micron) traces which were used for crosstalk control as well as impedance control. Figures 4-7 show close-up or more precise views of the dimensions of these signal line traces.

At the top of the loop, where the flip chip C4 connections are made, there is a parasitic capacitance caused by the ESD diodes as well as I/O transistor structures. With the given impedance levels of the bus, the present invention is able to generate a correction impedance that could cancel out up to 2.5 pf of capacitance. For example, the connections were reduced in width to the 35 micron (minimum) for a length of 3.2 mm to cancel out the 1.8 pf of parasitic capacitance on-chip.

Figure 4 shows an example of a close up view of the bus signal paths in Figure 3. It can be seen in this example that both the RSL traces and "buddy traces" are 35 um in width. The buddy traces act as electrical shields to intercept any crosstalk between adjacent